Docket No.: SON-2313
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Satoshi Ikeda

Confirmation No.: 3283

Application No.: 10/052,736

Art Unit: 2133

Filed: January 23, 2002

Examiner: J. C. Kerveros

For: SEMICONDUCTOR TESTING APPARATUS AND METHOD

REPLY BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is a Reply Brief under 37 C.F.R. §41.41 in response to the Examiner's Answer mailed on July 17, 2007.

In the Rejection mailed February 7, 2007, claims 3 and 6-32 were under 35 U.S.C. §102 as allegedly being anticipated by U.S. Patent No. 6,553,529 Reichert.

Subsequent to the rejection of February 7, 2007, an Amendment in Response to Non-Final Office Action has been filed concurrent with the Appeal Brief of July 17, 2007 for the purpose of cancelling claim 3. Accordingly, claims 6-32 are currently pending in this application, with claims 6 and 22 being independent.

No claims have been allowed.

All arguments presented within the Appeal Brief of July 17, 2007 are incorporated herein by reference. Additional arguments are provided hereinbelow.

Among others, the following positions were presented in the Examiner's Answer, each of which will be addressed in turn in this Reply Brief.

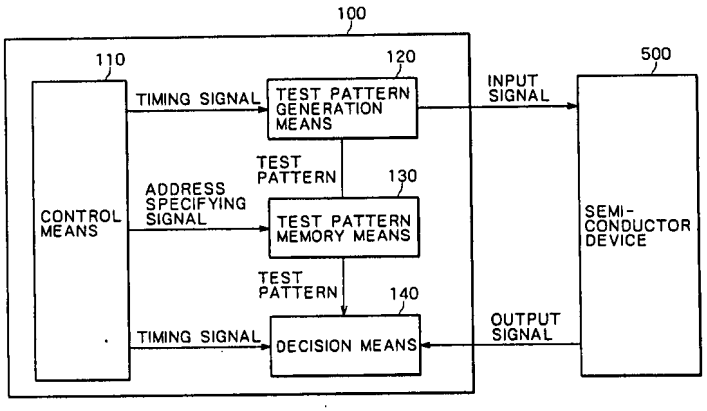
ARGUMENT

Generally - Throughout the Examiner's Answer are found various assertions regarding an interpretation of language found within the claims.

In response, the language found within the claims is both clear and unambiguous. The attempted reconstruction made within the Examiner's Answer is merely an attempt to redefine the invention in a manner different than from what is disclosed within the specification and set forth within the claims. Such an attempted reconstruction is without authority under Title 35 U.S.C., Title 37 C.F.R., the M.P.E.P. and relevant case law; such an attempted reconstruction is therefore deemed improper and inappropriate. See M.P.E.P. §2164.08.

The claims - Figure 1 of the specification as originally filed is provided hereinbelow.

FIG. 1



Control means 110 is adapted to generate a timing signal and an address specifying signal (specification at page 9, lines 11-16). The duration of said test pattern cycle period can be varied (specification at page 9, lines 16-20). The rate of modification for the address specifying signal is the test pattern cycle period (specification at figures 2, 3A, 3B, 3C, and 4).

The test pattern memory means 130 adapted to store a first test pattern, wherein the first test pattern is outputted from the test pattern memory means 130 in response to the address specifying signal (specification at page 10, lines 10-15). The rate of output for the first test pattern is the test pattern cycle period (specification at page 10, lines 13-15).

Test pattern generation means 120 is adapted to generate an input test pattern signal by combining the first test pattern with the timing signal (specification at page 10, lines 3-7). Moreover, semiconductor device under test 500 receives the input test pattern signal (specification at figure 1).

Reichert - Figures 1 and 2 of Reichert are provided hereinbelow.

FIG. 1

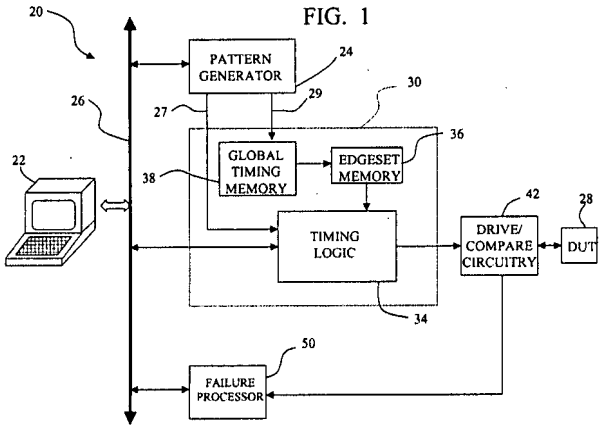


FIG. 2

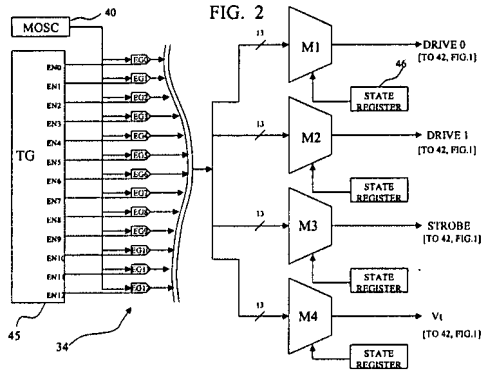
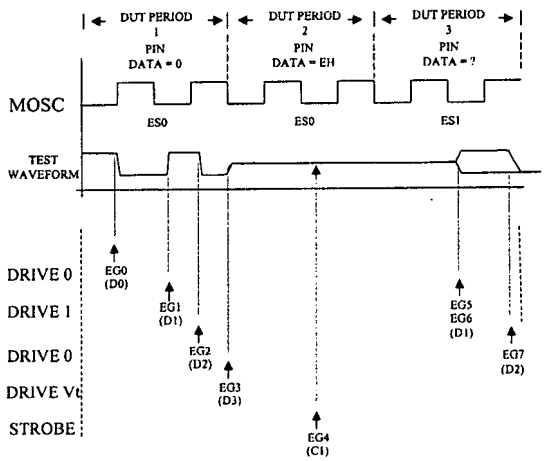


Figure 3 of Reichert is provided hereinbelow.

FIG. 3



Referring more particularly to Figure 2 of Reichert, the timing logic 34 according to one embodiment of the present invention, supports multi-modal testing of high and low-speed DUT pins by selectively providing timing values for assignment to desired user timings (Reichert at Figure 2, column 4, lines 46-50).

The timing logic preferably includes a programmable PLL-based master oscillator MOSC 40 and a timing generator 45 that provides respective enable inputs to a plurality of edge generators in the form of respective interpolators EG0-EG12 (Reichert at Figure 2, column 4, lines 50-53).

Page 11 of the Appeal Brief highlights that Reichert fails to disclose, teach, or suggest the timing logic 34 as being adapted to generate a timing signal and an address specifying signal.

In this regard, page 3 of the Examiner's Answer contends that Reichert teaches the *workstation 22* as being the claimed test pattern memory means.

Page 7 of the Examiner's Answer contends that each transition (or "edge") of the test waveform corresponds to one or more timing signals issued by one or more of the edge generators EG0-EG12 from the timing logic 34, where *each "EG" is equivalent to Appellant's specifying signal.*

In response, using the definition set forth within the Examiner's Answer that "*each 'EG' is equivalent to Appellant's specifying signal*", Reichert ***fails*** to disclose, teach, or suggest *the test controller 22* as being adapted to output a first test pattern ***IN RESPONSE*** to any of the edge generators EG0-EG12.

Instead, it is the *test controller 22* that automatically ***ASSIGNS*** *the edge generator* closest to the user-programmed timing (in this case for Drive 0, EG0) ***to fire*** while maintaining an acceptable level of accuracy (Reichert at column 7, lines 12-14).

Page 11 of the Appeal Brief highlights that Reichert fails to disclose, teach, or suggest the test controller 22 as being adapted to generate a timing signal and an address specifying signal.

In this regard, page 8 of the Examiner's Answer contends that evidently, Reichert's test controller 22 is capable of generating timing and control signals coupled to the pattern generation circuit 24 via system bus 26 capable of generating data and address signals on lines 27 and 29 coupled to the timing system 30 including the timing logic 34 for producing the programmed timing signals necessary to fire per-pin drive/compare circuitry 42.

In response, Reichert arguably teaches that for each event on each edgeset, the *test controller software* assigns an edge generator within the predetermined sub-group (Drive 0, Drive 1, Drive Vt, and Strobe) and programs it to the user-specified value (Reichert at column 5, lines 50-54).

However, Reichert fails to disclose, teach or suggest the *test controller 22* being capable ***of generating*** the timing signals (Drive 0, Drive 1, Drive Vt, and Strobe).

Instead, Reichert arguably teaches that the multiplexers respond to respective static registers 46 that are programmed at set-up time to, during operation, selectively pass *timing signals* to the drive/compare circuitry 42 (Reichert at column 5, lines 10-13). The *timing signals* correspond to actions "Drive to logic 0 (D0), "Drive to logic 1" (D1), strobe (C1) and "Drive to termination" (Vt) (Reichert at column 5, lines 13-15).

Page 12 of the Appeal Brief highlights that Reichert fails to disclose, teach, or suggest the pattern generation circuit 24 as being adapted to output a first test pattern in response to an address specifying signal generated by the control means, wherein the rate of output for the first test pattern is the test pattern cycle period; and

Page 12 of the Appeal Brief highlights that Reichert fails to disclose, teach, or suggest the test controller 22 as being adapted to output a first test pattern in response to an address specifying signal generated by the control means, wherein the rate of output for the first test pattern is the test pattern cycle period.

In this regard, pages 8-9 of the Examiner's Answer contend that the pattern generation circuit 24 is capable of generating test patterns including data and address signals on lines 27 and 29, respectively, in response to command and data signals generated from the test controller 22 routed via the system bus for controlling the pattern generation circuit for generating test pattern corresponding to a test waveform having a DUT period of operation, such as the test pattern cycle period, as shown in Fig. 3.

In response, page 7 of the Examiner's Answer contends that each transition (or "edge") of the test waveform corresponds to one or more timing signals issued by one or more of the edge generators EG0-EG12 from the timing logic 34, where *each "EG" is equivalent to Appellant's specifying signal.*

Reichert arguably teaches that an optional global timing memory circuit or timeset memory 38 couples to the *pattern generation circuit 24* via the global timeset address line 29 and feeds pre-programmed local timing data to the edgeset memory 36 to enable a reduction in

the memory capacity thereof (Reichert at column 4, lines 41-44). However, Reichert is **silent** as to the pattern generation circuit 24 as being adapted to output a first test pattern in response to "EG".

Moreover, a review of Figure 2 of Reichert reveals Reichert as failing to disclose, teach, or suggest "EG" being generated by the test controller 22. Furthermore, Reichert is **silent** as to the test controller 22 as being adapted to output a first test pattern in response to "EG". Instead, the timing logic preferably includes a programmable PLL-based master oscillator MOSC 40 and a *timing generator 45* that provides respective enable inputs to a plurality of edge generators in the form of respective *interpolators EG0-EG12* (Reichert at column 4, lines 50-54).

Page 13 of the Appeal Brief highlights that Reichert fails to disclose, teach, or suggest the failure processing circuit 50 as being adapted to detect a failure within the DUT 28 by comparing an output test pattern signal received from the DUT with the first test pattern outputted from the alleged test pattern memory means.

In this regard, page 9 of the Examiner's Answer includes an assertion that the location of the expected pattern *is not critical* in detecting a failure, since the failure processing circuit 50 is capable of detecting a failure by comparing the DUT output results with and expected pattern regardless of its location.

In response, Reichert arguably teaches the presence of a failure processing circuit 50 (Reichert at Figure 1, column 4, lines 22-25). The Final Office Action identifies an alleged pattern memory *within the computer workstation 22* of Reichert as the *test pattern memory means* (Final Office Action at page 6).

However, Reichert fails to disclose, teach, or suggest the failure processing circuit 50 comparing an output test pattern signal received from the DUT 28 with *the alleged pattern memory within the computer workstation 22*.

Page 13 of the Appeal Brief highlights that Reichert fails to disclose, teach, or suggest the computer workstation 22 as being adapted to vary said duration of said test pattern cycle period.

In this regard, page 9 of the Examiner's Answer includes urges that clearly, test controller 22 is capable of controlling the duration of the test pattern cycle period.

However, there is **nothing** within Reichert that teaches control of the ***duration of the test pattern cycle period***.

All arguments presented within the Appeal Brief are incorporated herein by reference.

CONCLUSION

The prior art of record, either individually or as a whole, fails to disclose, teach or suggest all the features of the claimed invention. For at least the reasons set forth hereinabove, the rejection of the claimed invention should not be sustained.

Therefore, a reversal of the rejection of February 7, 2007 is respectfully requested.

If any additional fee is required or any overpayment made, the Commissioner is hereby authorized to charge the fee or credit the overpayment to Deposit Account # 18-0013.

Dated: September 17, 2007

Respectfully submitted,

By_____
Ronald P. Kananen
Registration No.: 24,104
RADER, FISHMAN & GRAUER PLLC
Correspondence Customer Number: 23353
Attorney for Applicant